Millimeter-Wave Propagation within a Computer Chip Package

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Abstract—**Wireless Network-on-Chip (WNoC) appears as a promising alternative to conventional interconnect fabrics for chip-scale communications. The WNoC paradigm has been extensively analyzed from the physical, network and architecture perspectives assuming mmWave band operation. However, there has not been a comprehensive study at this band for realistic chip packages and, thus, the characteristics of such wireless channel remain not fully understood. This work addresses this issue by accurately modeling a flip-chip package and investigating the wave propagation inside it. Through parametric studies, a locally optimal configuration for 60 GHz WNoC is obtained, showing that chip-wide attenuation below 32.6 dB could be achieved with standard processes. Finally, the applicability of the methodology is discussed for higher bands and other integrated environments such as a Software-Defined Metamaterial (SDM).**

I. INTRODUCTION

Network-on-Chip (NoC) has become the paradigm of choice to interconnect cores and memory within a Chip MultiProcessor (CMP). However, recent years have seen a significant increase in the number of cores per chip and, within this context, it becomes increasingly difficult to meet the communication requirements of CMPs with conventional NoCs alone [1]. Their limited scalability is in fact turning communication into the next performance bottleneck in parallel processing and, therefore, new solutions are required to avoid slowing down progress in the manycore era [2].

Advances in integrated mmWave antennas [3]–[5] and transceivers [6], [7] have led to the proposal of Wireless Network-on-Chip (WNoC) as a potential alternative to conventional NoC fabrics [8]. In a WNoC, certain cores are augmented with transceivers and antennas capable of modulating and radiating the information. RF signals propagate through the computing package and can be demodulated by all tuned-in receivers. The main advantage of this approach is that distant cores can communicate with low latency as propagation occurs nearly at the speed of light. In fact, communication is naturally broadcast as long as antennas are roughly omnidirectional. Further, the lack of additional wires between cores provides system-level flexibility not achievable with other interconnects.

Due to its potential, WNoCs have been investigated extensively from the circuit [9], [10], link [11], [12], network [13], [14], and architecture perspectives [15], [16]. However, less attention has been paid to characterizing propagation within the computing package. Modeling the wireless channel is crucial to understand losses, dispersion, and multipath issues that impair communication and impact on the design and performance of the RF transceiver. For instance, the RF amplifiers contribute to more than half of the power consumption in WNoCs [10]. Therefore, quantifying channel attenuation becomes essential to optimize the cost of the wireless fabric.

This article investigates the wave propagation inside a realistic flip-chip package by means of EM simulation. We first provide a thorough description of the package and its influence on the antenna placement (Section II). Then, the S-parameters and the path loss over a mesh of 4×4 antennas are obtained at 60 GHz for three different integrated antennas (Section III). Through a parametric study, the design of the chip package is optimized to minimize losses and, thus, reduce the cost of wireless communication. Knowledge on the chip package also allows us to propose the space between bumps as a possible propagation channel at higher frequencies (Section IV).

To the best knowledge of the authors, this is the first comprehensive study assuming a realistic model of a flip-chip package and multiple mmWave antennas. Limited experimental measurements in a flip-chip package have been performed below 20 GHz [17], [18]. At higher frequencies, most works do not discuss the package properly [19]–[21] or assume wire bonding with the wire acting as antenna [22]. Little to no work has performed simulation-based explorations [21].

II. SYSTEM MODEL

This work models a flip-chip package with solder bumps for the channel characterization. During its manufacturing process, the solder bumps are deposited on the chip pads, which already carry a valid under bump metallization (UBM) like nickel/gold (Ni/Au). Then, the chip is flipped over and its solder bumps are aligned precisely to the pads of the package carrier external circuit. This is in contrast to wire bonding of chips on the package's carrier (or interposer, we use them interchangeably), in which the chip is mounted upright and wires are used to interconnect the chip pads to external circuitry [18].

Flip-chip packaging is oftentimes preferred over wire bonding for several reasons. First, the I/O signal inductance is much
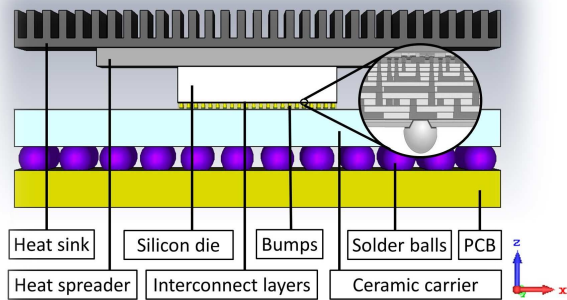
Fig. 1. Schematic of the layers of a flip-chip package

	Thickness	Material	ε_r	$\tan(\delta)$
Heat sink	0.5 mm	Aluminum	-	-
Heat spreader	0.25 mm	Thermal cond.	8.6	$3 \cdot 10^{-4}$
Silicon die	0.489 mm	Bulk Silicon	11.9	0.2517
Interconnections	13 µm	Cu and SiO_2	3.9	0.03
Bumps	87.5 µm	Cu and Sn	-	-
Ceramic carrier	0.5 mm	Alumina	9.4	$4 \cdot 10^{-4}$
Solder balls	0.32 mm	Lead	-	-
PCB	0.5 mm	Epoxy resin	4	-

lower due to its much shorter interconnect length, i.e. 100 µm or below [23] compared to 1–5 mm of the wire. The power–ground inductance is also small because the power is brought directly into the core of the silicon die instead of having to be routed to the edges. Further, this approach supports a higher power density since the whole die surface (not just the edges) is used. The edge space originally planned for wire bonding can, in fact, be eliminated to save space and silicon cost.

A. Structure of a flip-chip package

The layers are described from top to bottom following Fig. 1 and Table I. On top, the heat sink and heat spreader dissipate the heat out of the silicon chip, as they both have good thermal conductivity. Bulk silicon serves as the foundation of the transistors. This layer has low resistivity (10 Ω·cm), which is convenient for the operation of transistors, but not for electromagnetic propagation [21]. The interconnect layers, which occupy the bottom of the silicon die as shown in the inset of Fig. 1, are generally made of copper and surrounded by an insulator such as silicon dioxide (SiO_2) [3].

Very frequently, at the bottom of the interconnect layer, only over the chip I/O pads and being separated by chip passivation, a last UBM is provided (5µm Ni/80nm Au) to promote reliable solderability of the solder bumps [24]. On the last interconnect layer (13µm) and again over the I/O chip pads, the solder bumps are attached and, then, the chip is flipped and soldered to the underlying package carrier, which has on its top a very fine copper metallization external circuitry covered by a solder mask. At the specific pad openings on the ceramic carrier, which are aligned with the solder bumps of the flip chip package, a solderable metallization of also 5µm Ni/80nm Au or tin is applied as well. The choice of the carrier material is based on the match of its TCE with that of the silicon die. In this study, the package carrier is a 0.5-mm thick ceramic (other carriers could be epoxy-glass laminate, or silicon).

At the bottom of the ceramic carrier, an array of other solder balls (320 µm) is attached. These are essentially the interconnects of the flip-chip ceramic package with the underlying device PCB substrate, as shown in Fig. 1. The pitch of the solder balls is around one order of magnitude larger than those of the flip chip bumps. The constellation looks like a 2.5D flip chip on interposer or flip-chip ceramic Ball Grid Array (BGA), prior to its attachment on the device PCB substrate.

Although underfilling of the flip-chip bumps or the PCB solder balls is usually performed during manufacturing to increase the reliability of the end-device, such process does not influence our EM model and is considered out of the scope of this paper.

B. Antenna Placement

The placement of the antenna is discussed for an excitation at 60 GHz. A first option is to place the radiating element as far from the silicon as possible. This is proposed for printed dipoles in several works [4], [19], [25]. However, those works do not consider any package and, thus, are not affected by the bumps. In our case, we discard this option because waves would be blocked by the bumps, whose pitch is small compared to the wavelength of the antenna (100 µm to 1 mm).

A second option is to implement the radiating element in the metal layers closest to the silicon. Dipoles [18] or patch antennas [26] can be places in such layers. In the latter case, which is studied in this paper, the UBM and bumps act as ground plane while the insulator acts as the antenna substrate.

A third option is to add vertical Through-Silicon Vias (TSV) that act as monopole antennas. Advanced TSV and electroplating techniques [27] may allow to adjust the length of the via to make it resonant at the desired frequency. Vertical on-chip monopoles have been proposed recently [28], but using non-standard fabrication and packaging.

C. Types of antenna

The insets of Fig. 2 show the antennas used in this study. All antennas are tuned to 60 GHz ($|S11| < -10$dB).

Square aperture antenna. The aperture antenna is modeled as an electrically small waveguide port. It is not a realistic antenna due to the impossibility of building such an ideal aperture, but it serves the purpose of channel characterization as it has a quasi-isotropic radiation diagram. The antenna is placed horizontally within the SiO_2.

Patch antenna. The patch antenna is modeled as a planar metallic structure fed from one of the edges. The patch and its ground plane are implemented at the first and last metal layers of the structure. The SiO_2 serves as the antenna substrate.

Monopole antenna. The monopole antenna is modeled as a thin and long cylindrical metallic structure, placed vertically passing through the silicon and fed from the first metal layers. This creates a sort of *bed-of-nails* antenna distribution.

D. Simulation model

The structure shown in Fig. 1 is introduced in a full-wave solver. The dimensions and materials are as listed in Table
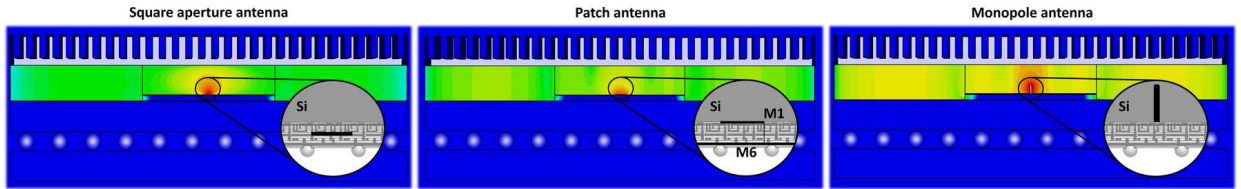
Fig. 2. Cross section of the electric field distribution for the three evaluated antennas, whose model is detailed in the insets.
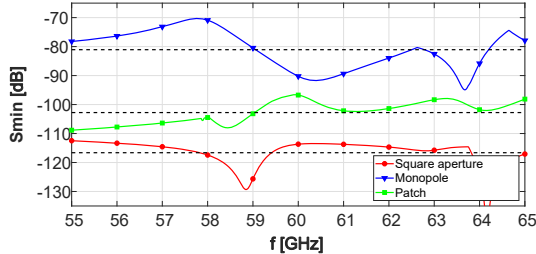

Fig. 3. Worst-case S-Parameter for each antenna. Dashed lines represent the mean over the 55–65 GHz band.

I. The lateral dimensions for the silicon chip and the flip-chip ceramic package are 22 mm and 33 mm, respectively, which are typical values in both research and industry. The interconnect layer stack (13 μm) is approximated by a SiO_2 layer under the silicon die and a copper layer over the solder bumps, while the antennas are placed either within the SiO_2 layer or through the silicon. Such approximation is driven by the rather large metal density close to the bumps and small lateral separation between the interconnects, which at 60 GHz is seen as a solid blocking element.

The full-wave solver allows to obtain the field distribution, the antenna gain, and the coupling between antennas. Then, the channel frequency response $H(f)$ is evaluated as

$$G_t G_r |H(f)|^2 = \frac{|S_{21}|}{(1 - |S_{11}|^2) \cdot (1 - |S_{22}|^2)}, \qquad (1)$$

where G_t and G_r are the transmitter and receiver antenna gain, S_{21} is the coupling between transmitter and receiver, whereas S_{11} and S_{22} are the reflection coefficients at both ends [29]. Once evaluated, a path loss analysis can be performed by fitting the attenuation over distance to

$$L_{dB} = 10n \cdot log_{10}(d) + C, \qquad (2)$$

where d is the distance between antennas and n is the path loss exponent [19]. The path loss exponent is around 2 in free space, below 2 in guided or enclosed structures, and above 2 in lossy environments.

III. SIMULATION RESULTS

We use CST [30] to obtain the field distribution and S-parameters in the 55–65 GHz band for a homogeneous distribution of 4×4 antennas within the package.

A. Antenna comparison

The field distribution for each type of antenna is shown in Fig. 2. It is observed that the field is confined at the region between the heat sink and the ceramic carrier. This is caused by the presence of several metallic blocks: heat sink on top, UBM at the bottom, and package walls on the side.

The aperture and patch, being planar, radiate mostly towards the heat sink and signals propagate laterally due to multiple reflections. On the other hand, the monopole has an azimuthal radiation pattern –most of the power propagates laterally.

Fig. 3 plots the worst-case coupling S_{min}, which is the minimum S-parameter between any antenna pair

$$S_{min}(f) = \min_{i,j \neq i} S_{ij}(f), \qquad (3)$$

as well as the average value over the whole band. The results show that, in consonance with the field distribution analysis, the monopole has the best coupling among the considered alternatives (-81.1 dB). The coupling between patches is, as expected, higher than for the electrically small –and therefore inefficient– aperture antenna. In all cases, the very large attenuation is mostly due to the presence of lossy silicon.

The standard deviation of S_{min} over frequency is also evaluated. A low value is preferred as it implies a larger effective bandwidth. High values are due to notches produced by either the resonant nature of the antennas or multipath effects. The monopole and the patch yield the highest (6.03 dB) and lowest value (3.66 dB), suggesting the existence of an interesting efficiency–bandwidth tradeoff among antennas.

B. Package design

The attenuation values obtained above need to be greatly improved to consider intra-chip wireless as a viable and efficient option. Package co-design techniques that may help to address this issue are explained and evaluated next.

Additional dielectric layer. By considering the field distribution results above and basing on other studies [17], [20], a good way to reduce propagation losses is to make use of the heat spreader as it generally has low electrical losses [21]. Silicon carbide, beryllium oxide and aluminum nitride (AlN) are widespread due to their excellent thermal properties; in this study, AlN is chosen as it has the lowest electrical losses.

Simulations are repeated for different AlN thicknesses. As observed in Fig. 4(a), increasing the AlN thickness improves the average S_{min} up to 33 dB with respect to not having AlN. Although not shown here, it is worth noting that the standard deviation of S_{min} oscillates (not uniformly) between 2.7 and 8.2 dB. Therefore, it is a parameter to take into account when selecting the AlN thickness.

Thinning the silicon. The characteristics of the bulk silicon suggest that most losses occur in it. Consequently, reducing the silicon thickness is an intuitive way to minimize the losses as it shortens the propagation through the silicon layer. Furthermore, the radiation efficiency of the antennas increases as the near-field influence of the lossy silicon die is minimized.
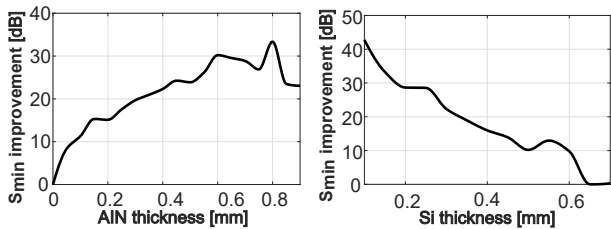
(a) Improvement over no AIN (b) Improvement over 0.7-mm Si

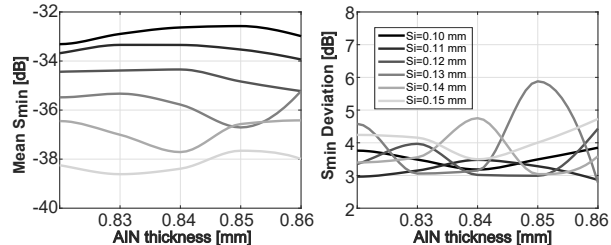Fig. 4. Average coupling enhancement for different AIN and Si thicknesses.

Fig. 5. Mean and standard deviation of the worst-case coupling for several silicon and AIN thicknesses.

Fig. 6. Path loss for each antenna pair and log-distance fitting.

Fig. 7. Field distribution along the X-axis within the bump region.

To quantify these effects, simulations are repeated by considering silicon thicknesses down to 100 μm, although chip makers can reportedly reduce that further to tens of microns [31]. As we can see in Fig. 4(b), the path loss difference between the 0.1mm and 0.7mm cases is over 40 dB. The standard deviation oscillates between 2.9 and 6.6 dB and shall be considered when designing the package.

Antenna and package co-design. Previous results have provided a choice for the antenna, as well as rough dimensions for the silicon and heat spreader layers that minimize the path loss. To provide a design point that adds up the benefits of the three processes, we perform an antenna-package co-design optimization. We explore the design space around the optimal silicon and AIN thicknesses by keeping the monopole matched at 60 GHz at all times. This is important because the effective wavelength of the antenna slightly varies among cases.

Fig. 5 shows the results of the parametric design-oriented study. It is found that the optimal silicon and AIN thicknesses are 0.10 mm and 0.85 mm, respectively, as they yield the highest mean with low variance. In summary, the optimization process has reduced the losses from 81.1 dB to only 32.6 dB.

C. Path loss analysis

We next evaluate the path loss exponent for the optimal case found with the antenna-package co-design. The channel response is computed for every antenna pair using Eq. (1) assuming identical gains in transmission and reception. The attenuation at 60 GHz is plotted as a function of the distance between antennas and a linear regression fitting is performed with distance in a logarithmic scale. Fig. 6 shows the results: a line with a slope of 9.32 dB/mm is obtained, which means that the path loss exponent is $n = 0.932$. This is significantly lower than the freespace exponent ($n = 2$) and the exponent obtained in [19] for on-chip mmWave propagation without a chip package ($n \approx 1.4$). This result stresses the importance of the enclosed nature of the package and its waveguiding effect.
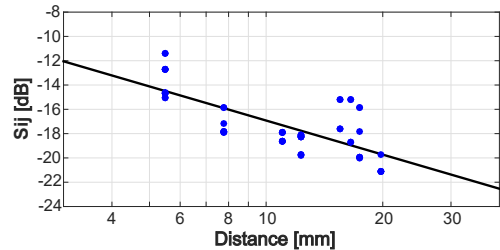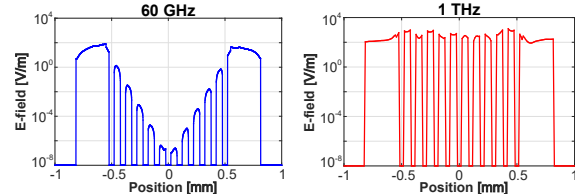
IV. DISCUSSION

Other scenarios. The methodology of this work is applicable to new relevant scenarios such as System-in-Package (SiP) or Software-Defined Metamaterials (SDM). In a SiP [32], several flip chips can be assembled on the ceramic carrier, making the package more of an integration platform for heterogeneous functionalities (e.g., CPU+GPU). In a SDM [33]–[35], a network of controllers are co-integrated below a metasurface to provide EM programmability. Both scenarios shall incorporate the effect of the added components into the EM model.

Scaling in frequency. The location of the antennas in this work has been motivated by the small pitch of the bumps. The blocking effect of the bumps is observed in the left plot of Fig. 7 as the electric field along the X-axis decays several orders of magnitude in the space between bumps (it is null within them). As the wavelength becomes commensurate to the pitch, however, one would expect bumps to no longer be an obstacle. This is confirmed in the right plot of Fig. 7, which assumes an excitation at 1 THz (∼100 μm) and shows strong fields in the center of the die. This suggests that as CMOS or graphene-based THz technologies become available [36]–[38], propagation through the bumps region should be considered.

V. CONCLUSIONS

In this work, we performed a simulation-based study of wave propagation within a realistic flip-chip ceramic BGA package. Among the evaluated antennas, the vertical monopole delivered higher coupling. It has been also demonstrated that by thinning the lossy silicon and using the heat spreader as propagation layer, losses between monopole antennas can be reduced by ∼50 dB. The path loss analysis yielded an exponent of 0.9, which confirms that the waveguide effect is dominant in this environment. Finally, it has been suggested that inter-bump propagation could be feasible at THz frequencies and should be considered in emerging applications.

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